

ABSTRACT OF THE DISCLOSURE

An error rate select circuit activated in an information sustaining mode is provided, wherein a plurality of pieces of data are read from a dynamic memory circuit and inspection bits which are used to detect an error existing in the pieces of data are generated. If no error is detected, a first predetermined value is added to a total value. If an error is detected, a second predetermined value greater than the first predetermined value is subtracted from the total value. If the total value exceeds a first set value, a refresh period is lengthened by a predetermined time increment. If the total value becomes smaller than a second set value, the refresh period is shortened by the predetermined time increment.